



1/13 inch QVGA CMOS Image Sensor

BF3901UCS

Datasheet



Content

1. GENERAL DESCRIPTION.....	3
2. FEATURES.....	3
3. APPLICATIONS.....	4
4. TECHNICAL SPECIFICATIONS.....	4
5. FUNCTIONAL OVERVIEW.....	5
5.1 PIXEL ARRAY.....	6
5.2 COLUMN CDS.....	7
5.3 TIMING CONTROLLER.....	7
5.4 ANALOG SIGNAL PROCESSOR.....	7
5.5 A/D CONVERTER.....	7
5.6 AUTOMATIC BLACK CONTROL.....	7
5.7 IMAGE SIGNAL PROCESSOR.....	7
6. SPECIFICATIONS.....	8
6.1 ELECTRICAL CHARACTERISTICS.....	8
6.1.1. <i>Absolute Maximum Ratings</i>	8
6.1.2. <i>DC Parameters</i>	8
6.1.3. <i>Clock Requirement</i>	9
6.2 ELECTRO-OPTICAL CHARACTERISTICS.....	9
6.3 INPUT-OUTPUT AC CHARACTERISTICS.....	10
7. TWO-WIRE SERIAL INTERFACE& REGISTER.....	12
7.1 THEORY OF OPERATION.....	12
7.2 TWO-WIRE SERIAL INTERFACE FUNCTIONAL DESCRIPTION.....	13
7.3 REGISTER SUMMARY (FULL LIST).....	14
8. PACKAGE SPECIFICATIONS.....	24

1. General Description

The BF3901UCS is a highly integrated QVGA camera chip which includes CMOS image sensor (CIS) and image signal processing function (ISP). It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity and very low power consumption imaging system. The sensor consists of a 248 x 328 effective pixel array which has an optical format of 1/13 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, automatic black level compensation and on-chip 10-bit ADC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB444, RGB555, RGB565, YCbCr 4:2:2. It has a commonly used two-wire serial interface for the host to control the operation of the whole sensor.

The product is capable of operating at up to 30 frames per second at 24MHz clock in QVGA mode, with complete user control over image quality and data format. All required image processing functions, including exposure control, and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/13 inch.
- 30 frame/sec QVGA mode @ 24MHz master clock.
- Ultra-low dark noise at high temperature.
- Various output formats: YCbCr 4:2:2, RGB444, RGB555, RGB565, Raw Bayer(248 x 328).
- Power supply: 2.7~3.0V for core, 1.7~3.0V for I/O.
- Horizontal /Vertical mirror.
- 50/60Hz flicker cancellation.
- Programmable I/O drive capability.
- Automatic black level control.
- Image processing function: Lens Shading Correction, Gamma Correction, Bad Pixel Correction, Color Interpolation, False Color Suppression, Purple Fringe Correction, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation and Contrast, and Data Format Conversion.
- 12 types of special video effect
- On-chip test pattern generation of many types including customer programmable
- Package: CSP, Bare Die

3. Applications

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Video telephony and conferencing equipments
- Surveillance systems
- Industrial and medical systems

4. Technical Specifications

- Active pixel array: 248 x 328
- Pixel size: 3.15 μ m×3.15 μ m
- Sensitivity: 4.8V/lux.s
- Dark current: 2.5 mV/S at 40°C
- Power consumption: 32mW @ 30fps and single 2.8V supply
- Standby current: TBD
- S/N Ratio: 45dB
- Dynamic range: 61dB
- Operating temperature: -20~60°C
- Stable Image temperature 0~50°C
- Optimal lens chief ray angle: 25°

5. Functional Overview

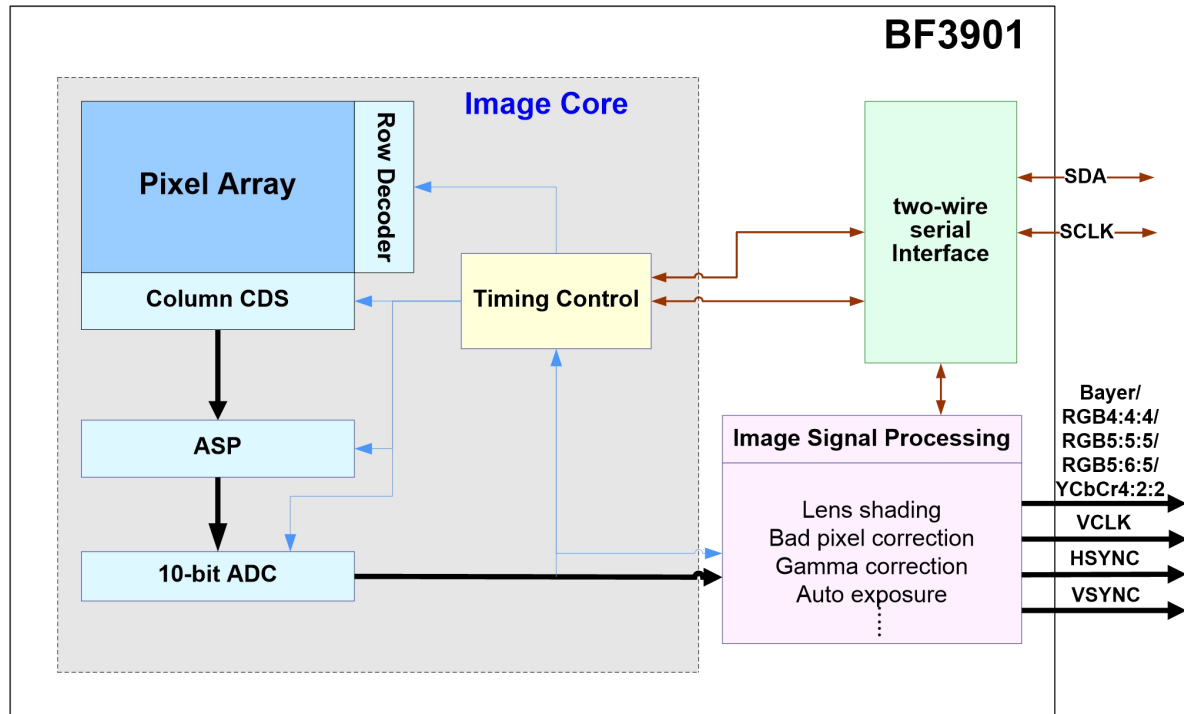


Figure 1. Block Diagram

BF3901UCS has an active image array of 248 x 328pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

5.1 Pixel Array

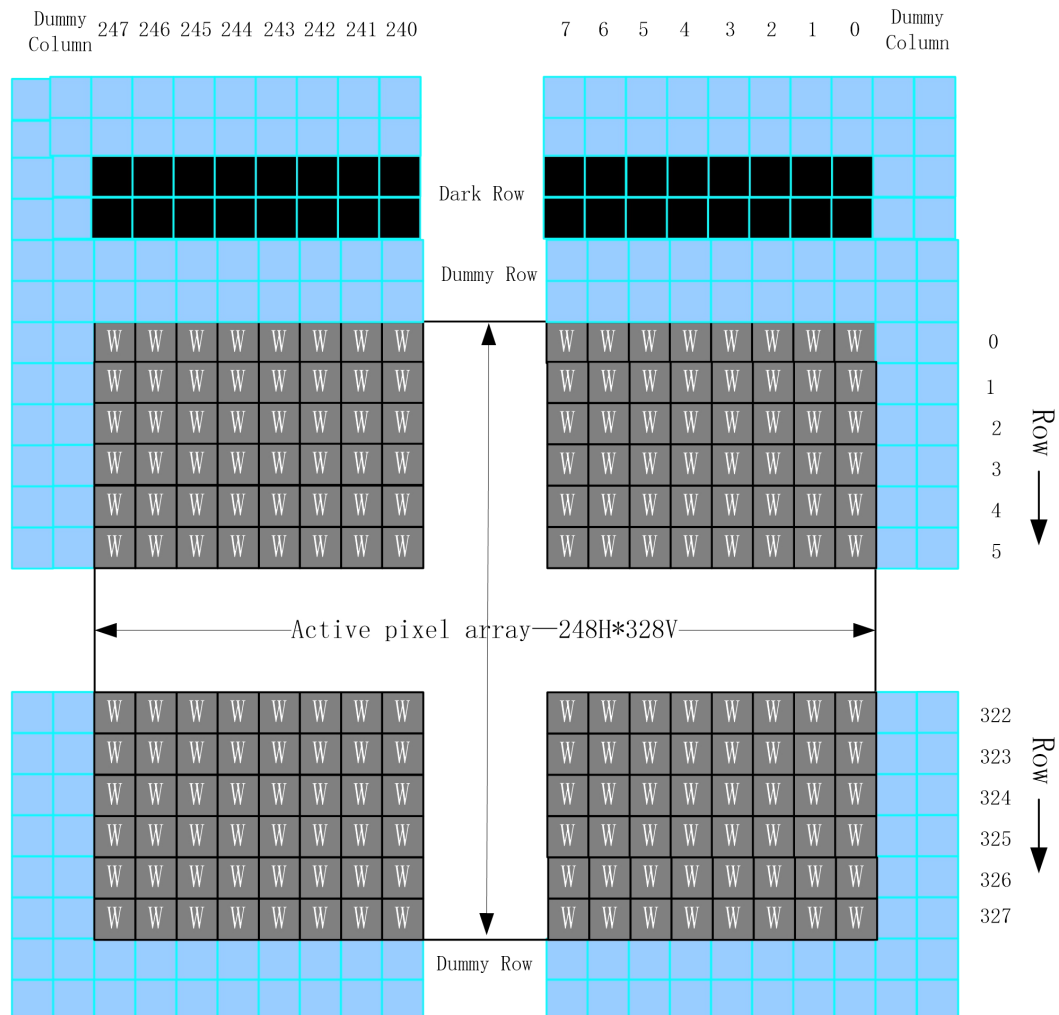


Figure 2. Sensor Array Region

The active pixel array is configured as 248 columns by 328 rows. Dummy pixels and dark rows are added outside the active pixel array.

Pixel array is not covered by Bayer color filters as can be seen in the figure2. Since each pixel unit is not covered with a color filter,each pixel can obtain all the information.BF3901UCS can provide the Raw Bayer data or YUV data through an 1 or 2-bit SPI output data bus. If no flip in column, column is read out from 0 to 247. If flip in column, column is read out from 247 to 0. If no flip in row, row is read out from 0 to 327. If flip in row, row is read out from 327 to 0. In this way, the output pixel color order is always the same.

5.2 Column CDS

BF3901UCS has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Timing controller

The timing controller controls the following functions

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- External timing outputs (VSYNC, HREF and VCLK)

5.4 Analog Signal Processor

This block performs all analog image functions including Color gain/Global gain control and black level compensation.

5.5 A/D converter

The analog signals are converted to digital forms column by column and row by row, through out the whole array. BF3901UCS provides the 10-bit Raw Bayer data for ISP through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, False Color Suppression, Low Pass Filter, Color Space Conversion, Edge Enhancement, Auto exposure, Contrast, and Data Format Conversion.

6. Specifications

6.1 Electrical Characteristics

6.1.1. Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.0 V
- Supply voltage (VDD3A): 2.7 ~ 3.0 V
- Operating temperature: -20~60 °C
- Storage temperature: -30~80 °C
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2. DC Parameters

Table 1. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	2.8	3.0	
VDD3A	Analog power supply	V	2.7	2.8	3.0	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	10.0	--	1
I_vdd3a	VDD3A supply current, normal operation mode	mA	--	10.0	--	2
Vih	Input voltage logic "1"	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic "0"	V	--	--	0.2*VDDIO	--
Voh	Output voltage logic "1"	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic "0"	V	--	--	0.1*VDDIO	--

Note:

1. Because power consumption of I/O depends on the output load and system environment, user should supply enough current to sensor for stable operation. It is measured when output load is floated.
2. Because current of analog circuit depends on the registers' values, it is measured at specific register's value.

6.1.3. Clock Requirement

Table 2. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
MCLK	Main clock frequency	MHz	6	48	--	1
SCLK	two-wire serial interface clock frequency	KHz	--	400	--	2
Inormal	Current in YUV4:2:2 output mode	mA	--	20	--	3
Idown	Current in power down mode	uA	--	30	--	4

Note:

1. XCLK(external clock) may be divided by internal clock division logic to get MCLK for easy integration with high speed video codec system.
2. SCLK is driven by host processor. For the detail serial bus timing, refer to two-wire serial interface section
3. VDDIO=2.8V, VDD3A=2.8V(YUV4:2:2 output).
4. Hardware power down.

6.2 Electro-Optical Characteristics

Clock frequency: 24MHz.

Operating voltage: VDDIO=2.8V, VDD3A=2.8V.

Operating temperature: 25°C

Table 3. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	4.8		1
Dark current	mV/sec	--	3	6	2
S/N ratio	dB	--	45	--	--
Dynamic Range	dB	--	61	--	--
Frame Rate	fps	--	--	30	3

Notes:

1. Measured at 50 lux white light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (40 Celsius).
3. With 240×320 size at MCLK 48MHz.

6.3 Input-Output AC Characteristics

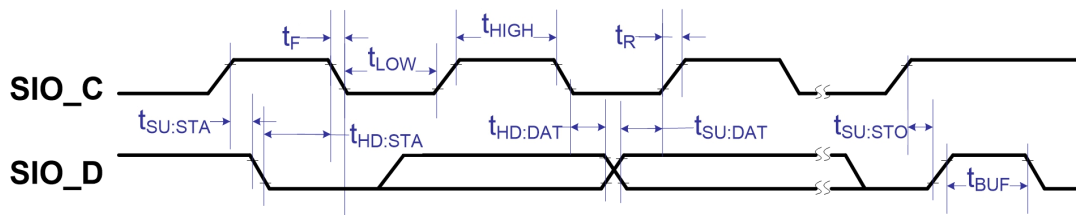


Figure 3. Two-Wire Serial Interface Timing

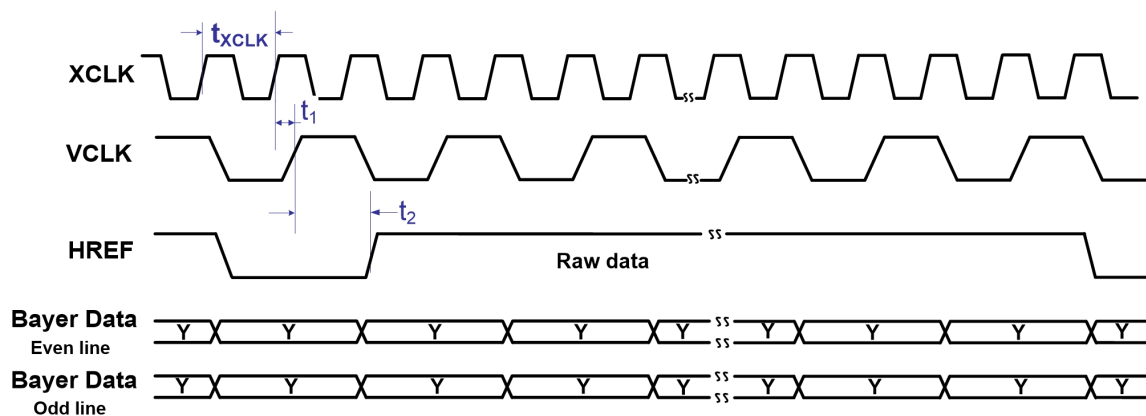


Figure 4. Horizontal Timing Raw Bayer Data

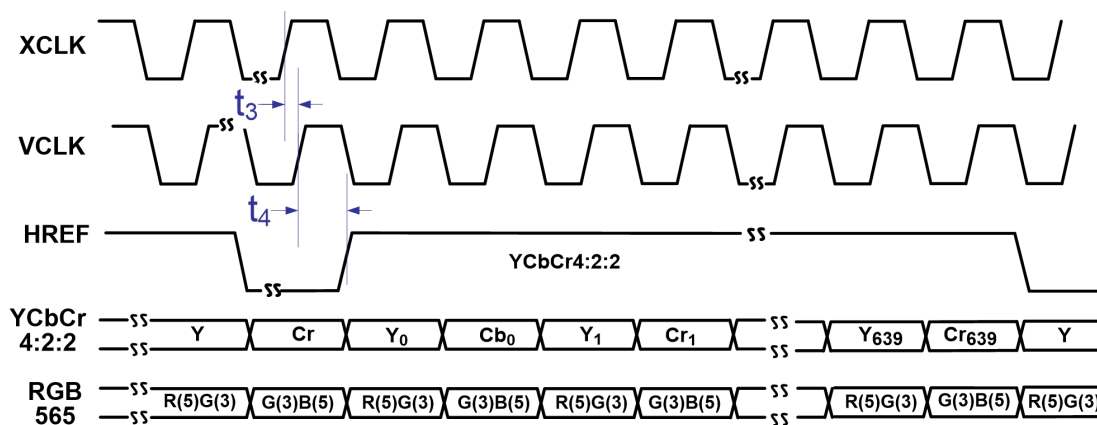


Figure 5. Horizontal Timing YUV4:2:2

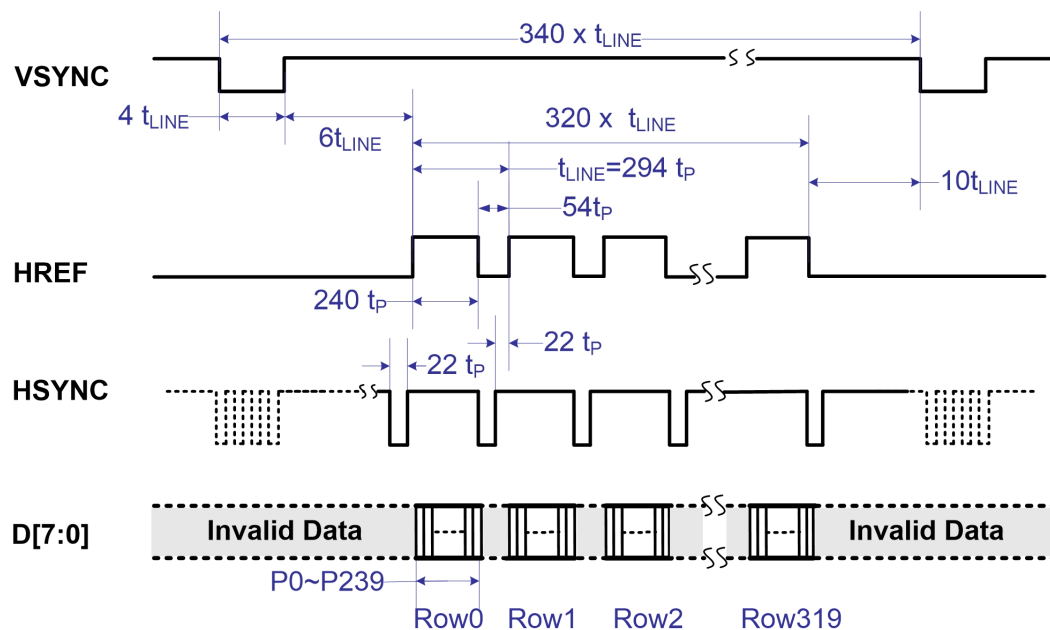


Figure 6. QVGA YUV Frame Timing

Table 4. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	$t_P = 2 \times t_{MCLK}$	--	41.6	--	ns
f_{MCLK}	Master Clock Frequency	--	48	--	MHz
f_{VCLK}	Video Clock Frequency for Raw data , $f_V = f_{MCLK} / 2$ for YUV/RGB , $f_V = f_{MCLK}$	--	24/48	--	MHz
t_{LINE}	Line length	--	$294 \times t_P$	--	ns
t_R, t_F	two-wire serial interface rise/fall times	--	--	300	ns
t_{LOW}	Clock Low Period	1.3	--	--	us
t_{HIGH}	Clock High Period	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns
t_1	XCLK rising to VCLK (RAW DATA)	--	10	--	ns
t_2	VCLK to HREF (RAW DATA)	--	10	--	ns
t_3	XCLK rising to VCLK (YUV)	--	17	--	ns
t_4	VCLK to HREF (YUV)	--	10	--	ns

7. Two-wire serial interface& Register

7.1 Theory of Operation

The registers of BF3901UCS are written and read through the two-wire serial interface. BF3901UCS has two-wire serial interface slave. BF3901UCS is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out of BF3901UCS through the two-wire serial interface data (SDA) line. The SCLK and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: *Two-wire serial interface device address of BF3901UCS is 6eh.*

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” in the LSB of the address indicates write mode, and “1” indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where "0" indicates write and "1" indicates read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF3901UCS uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

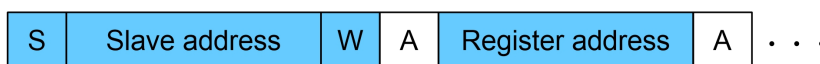
Single Write Mode Operation



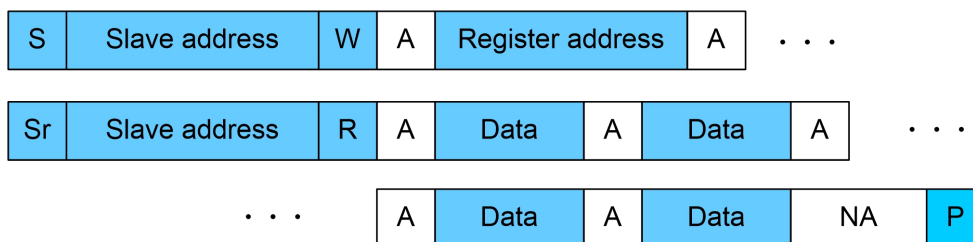
Multiple Write Mode (Register address is increased automatically) ¹ operation



Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) ¹ Operation



From master to slave



From slave to master

S: Start condition.

Sr: Repeated Start (Start without preceding stop.)

Slave Address:

write address = DCh = 11011100b

read address = DDh = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit.

NA: No Acknowledge.

Data: 8-bit data

P: Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically.
If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 Register Summary (full list)

Table 5. BF3901UCS all registers

Address	Name	Width	Default value	Description
01h	BLUE_GAIN	6	19h	Blue gain.
02h	RED_GAIN	6	15h	Red gain.
03h	VHREF	8	00h	VREF and HREF Control, Bit[7:4]: Reserved; Bit[3]: VREF end low 1 bit (high 8 bits at VSTOP[7:0]); Bit[2]: VREF start low 1 bit (high 8 bits at VSTART[7:0]); Bit[1]: HREF end low 1 bit (high 8 bits at register HSTOP[7:0]); Bit[0]: HREF start low 1 bit (high 8 bits at register HSTART[7:0]).
09h	COM2	8	10h	Common Control 2, Bit[7:6]: Vclk Output Drive Capability, 00: 1x, 01: 1.5x, 10: 2.5x, 11: 3x; Bit[5]: Reserved; Bit[4]: Standby Mode, 0: Disable standby mode, 1: Enable standby mode; Bit[3:2]: Hsync Output Drive Capability, 00: 1x, 01: 1.5x, 10: 2.5x, 11: 3x; When 0x20[6]=0, Bit[1:0]: Data & VCLK & HSYNC Output Drive Capability, 00: 1x, 01: 1.5x, 10: 2.5x, 11: 3x; When 0x20[6]=1, Bit[1:0]: Data Output Drive Capability, 00: 1x, 01: 1.5x, 10: 2.5x, 11: 3x.

0ah	COM5	8	11h	Common Control 5, Bit[7:4]: Total columns number (M1) for gate subsample; Bit[3:0]: Columns selected number (M2) for gate subsample. Note: Set M3(Set by register COM8[3:0]) columns to a package, and select M2 columns from M1 columns.
0bh	COM4	8	00h	Common Control 4, Bit[7]: Row Selected in CK-GATE Mode, 0: Select even row, 1: Select odd row; Bit[6]: Column Selected in CK-GATE Mode, 0: Select even column, 1: Select odd column; Bit[5]: 0: Output normal HSYNC/VSYNC, 1: Output fixed value: HSYNC=HSYNC_VAL,VSYNC=VSYNC_VAL; Bit[4]: The Fixed Value of Output HSYNC and VSYNC, 0: HSYNC_VAL=VSYNC_VAL=0, 1: HSYNC_VAL=VSYNC_VAL=1; Bit[3:0]: Reserved.
0ch	COM3	8	00h	Common Control 3, Bit[7]: Processed Raw Data Control, 0: Processed raw data from YCbCr to RGB conversion in DATFORMAT module, 1: Processed raw data from color interpolation (Processed by Lens Shading Correction, Gamma Correction, Bad Pixel Correction, Cluster Correction, and De-noise); Bit[6]: Output data MSB and LSB swap; Bit[5:4]: Output Processed Raw Data Order (when 0x0c[7]=0), 00: (LINE0: BGBG/LINE1: GRGR), 01: (LINE0: GBGB/LINE1: RGRG), 10: (LINE0: GRGR/LINE1: BGBG), 11: (LINE0: RGRG/LINE1: GBGB); Bit[3]: 0: No HREF when VSYNC_DAT signal is low, 1: Always has HREF no matter VSYNC_DAT is low or not; Bit[2]: DATA Control, 0: Normal, 1: DATA is ahead of HREF 1 clk (YUV MCLK, Raw Data PCLK); Bit[1:0]: HREF Control, 00: Normal, 01: HREF is ahead of DATA 0.5 clk (YUV MCLK, Raw Data PCLK), 10: HREF is ahead of DATA 1 clk (YUV MCLK, Raw Data PCLK), 11: HREF is ahead of DATA 1.5 clk (YUV MCLK, Raw Data PCLK).
0eh	DBLK_TAR_EG	8	10h	Black control target for G1.
0fh	AVER_OR	8	10h	Read out black aver for R. Read Only.
10h	COM6	8	11h	Common Control 6, Bit[7:4]: Total rows number (N1) for gate subsample; Bit[3:0]: Rows selected number (N2) for gate subsample. Note: Set N3 rows (set by register COM8 [7:4]) to a package, and select N2 rows from N1 rows.
11h	CLKRC	8	30h	MCLK Division Control, Bit[7]: Double Clock Option, 0: Disable double clock option, meaning the maximum MCLK can be as high as half input clock, 1: Enable double clock option, meaning the maximum MCLK can be as high as input clock; Bit[6]: Use external clock directly (F(internal clock)=F(input clock)); Bit[5:4]: Mclk divider factor, 00: Divided by 1, 01: Divided by 2, 10: Digital power down, 11: Divided by 4; Bit[3:0]: Reserved.

12h	COM7	8	20h	Common Control 7, Bit[7]: SCCB Register Reset, 0: No change, 1: Resets all registers to default values; Bit[6]: Reserved; Bit[5]: Zhan Xun or MTK CCIR Swap Control, 1: Swap, 0: No swap; Bit[4]: Zhan Xun or MTK CCIR Selection Control, 1: Select Zhan Xun CCIR, 0: Select MTK CCIR; Bit[3]: Reserved; Bit[2]: YUV422/RGB565/RGB555/RGB444 Selection; Bit[1]: 1: Change data 0x00 to 0x01, and change data 0xff to 0xfe, 0: Normal data; Bit[0]: Raw RGB Selection, {0x12[2], 0x12[0]} 00: YUV422, 01: Raw Data, 10: RGB565/RGB555/RGB444(used with 0x3a), 11: Processed Raw Data(used with 0x0c[7]).
13h	COM8	8	c7h	Common Control 8, Bit[7:4]: Reserved; Bit[3]: Page switch; Bit[2]: AGC Enable, 0: Disable, 1: Enable; Bit[1]: Reserved; Bit[0]: AEC Enable, 0: Disable, 1: Enable.
15h	COM10	8	02h	Common Control 10, Bit[7]: Reserved; Bit[6]: 0: Output HREF, 1: Output HSYNC; Bit[5]: 0: Output VSYNC_IMAGE, 1: Output VSYNC_DAT; Bit[4]: VCLK reverse; Bit[3]: HREF option, 0: Active high, 1: Active low; Bit[2]: Reserved; Bit[1]: VSYNC option, 0: Active low, 1: Active high; Bit[0]: HSYNC option, 0: Active high, 1: Active low.
17h	HSTART	8	00h	Output Format-Horizontal Frame (HREF column) start high 8-bits (low 1bit is at VHREF[0]).
18h	HSTOP	8	78h	Output Format-Horizontal Frame (HREF column) end high 8-bits (low 1 bit is at VHREF[1]).
19h	VSTART	8	00h	Output Format-Vertical Frame (row) start high 8-bits (low 1 bit is at VHREF[2]).
1ah	VSTOP	8	a0h	Output Format-Vertical Frame (row) end high 8-bits (low 1 bit is at VHREF[3]).
1bh	PLLCTL	8	80h	PLL Control, Bit[7]: PLL Enable, 0: Enable, 1: Disable; Bit[6:3]: Reserved; Bit[2]: Output Clock Division, 0: Divided by 8, 1: Divided by 4; Bit[1:0]: Input Clock Division, 00: Divided by 1, 01: Divided by 2, 1x: Divided by 4;
1ch	MIDH	8	7fh,RO	Manufacturer ID MSB.
1dh	MIDL	8	a2h,RO	Manufacturer ID LSB.
1eh	MVFP	8	09h	Mirror/Vertical Flip Control, Bit[7]: Control the analog GLB_GAIN delay a frame or not; Bit[6]: Reserved; Bit[5]: Mirror 0: Normal image, 1: Mirror image; Bit[4]: Vertical Flip 0: Normal image, 1: Vertically flip image; Bit[3:0]: Control the rising edge of PRST.
1fh	DBLK_TAR_EB	8	10h	Black control target for B.

20h	TDREG	8	09h	Bit[7]: Reserved; Bit[6]: HSYNC & VCLK Pad Drive Capability Control, 0: Same drive capability, 1: Drive capability adjustment independently; (Refer to register COM2) Bit[5:0]: Reserved.
22h	DBLK_TAR_OG	8	10h	Black control target for G2.
23h	GLGAINREG	7	33h	Green Gain[2:0], Bit[6:4]: G1 Gain (used as GreenEgain[2:0]); Bit[2:0]: G2 Gain (used as GreenOgain[2:0]).
24h	AE_TAR1	8	41h	Bit[7]: Reserved; Bit[6:0]: AE target value.
25h	AE_LOC	8	88h	COM8[3] 0: Bit[7:4]: AE Lock1; Bit[3:0]: AE Lock2; COM8[3] 1: Bit[7:0]: P_PIXEL_OE.
26h	DBLK_TAR_OR	8	10h	Black control target for R.
2ah	EXHCH	8	00h	Dummy Pixel Inserted MSB, Bit[7:4]: Dummy pixel inserted in horizontal direction 4 MSB; Bit[3:0]: Reserved.
2bh	EXHCL	8	06h	Dummy Pixel Inserted LSB, Dummy pixel inserted in horizontal direction 8 LSB.
2ch	AVER_EB	8	10h	Read out black aver for B. Read Only.
2dh	AVER_EG	8	10h	Read out black aver for G1. Read Only.
2eh	AVER_OG	8	10h	Read out black aver for G2. Read Only.
30h	HSYST	8	28h	Used to control the rising edge of HSYNC 8 LSB, (The high 4 bits at H_HSYNC_EDGE[7:4]).
31h	HSYEN	8	14h	Used to control the falling edge of HSYNC 8 LSB, (The high 4 bits at H_HSYNC_EDGE[3:0]).
33h	OFFSET	8	10h	Auto offset for lens shading correction (the same as black_aver).
34h	OFFSET_REG	8	1dh	Manual written offset for lens shading correction.
35h	R_COEF	8	46h	Lens shading correction gain for R pixel.
36h	OFFSET_MODE GAIN_SEL YOH_G YOH_B	8	40h	Bit[7]: OFFSET_MODE, 0 : Use auto offset for lens shading correction, 1 : Use manual written offset for lens shading correction; Bit[6]: Reserved; Bit[5]: The vertical center high 1 bit of G(vertical center); Bit[4]: The vertical center high 1 bit of B(vertical center); Bit[3:0]: Reserved.
37h	YOL_B	8	a4h	The vertical center low 8 bits of B (vertical center).
38h	XOL_B	8	7ch	The horizontal center low 8 bits of B (horizontal center).
39h	MAN_OFFSET OFFSET_ME	8	90h	Bit[7]: Gamma Offset Control1 0: Auto offset1, 1: Manual offset1; Bit[6:0]: The manual written gamma offset.

3ah	TSLB	8	00h	Data Output Sequence, Bit[7]: 1: DATA counter delay one sclk, 0: No delay (for SPI or four bits mode); If YUV422 is selected, the Sequence is: Bit[1:0]: Output YUV422 Sequence, 00: YUYV, 01: YVYU, 10: UYVY, 11: VYUY; If RGB565/RGB555/RGB444 is selected, the Sequence is: Bit[4:0]: Output RGB565/RGB555/RGB444 Sequence, RGB565: 00h: R5G3H,G3LB5, 01h: B5G3H,G3LR5, 02h: B5R3H,R2LG6, 03h: R5B3H,B2LG6, 04h: G3HB5,R5G3L, 05h: G3LB5,R5G3H, 06h: G3HR5,B5G3L, 07h: G3LR5,B5G3H, 08h: G6B2H,B3LR5, 09h: G6R2H,R3LB5; RGB555: 0Ah: 1'b0R5G2H,G3LB5, 0Bh: G3LB5,1'b0R5G2H, 0Ch: R5G3H,G2LB51'b0, 0Dh: G2LB51'b0, R5G3H, 0Eh: B5G3H,G2L1'b0,R5, 0Fh: R5G3H,G2L1'b0,B5, 10h: B51'b0G2H,G3LR5, 11h: R51'b0G2H,G3LB5; RGB444: 12h: 4'b0R4,G4B4, 13h: G4B4,4'b0R4, 14h: 4'b0B4,G4R4, 15h: G4R4,4'b0B4, 16h: R4G4,B44'b0, 17h: B44'b0,R4G4, 18h: B4G4,R44'b0, 19h: R44'b0,B4G4, 1Ah: B4G4,R4B4, 1Bh: R4G4,B4R4, 1Ch: R4G2H2'b0,G2LB42'b0, 1Dh: B4G2H2'b0,G2LR42'b0, 1Eh: B41'b0G3H,G1L2'b0R41'b0, 1Fh: R41'b0G3H,G1L2'b0B41'b0; Bit[6:5]: Reserved.
3dh	COM11	8	11h	Common Control 11, Bit[7:4]: Total rows number(M3) for gate subsample, Bit[3:0]: Total columns number(N3) for gate subsample.
3eh	TAREG2	8	03h	Bit[7]: Tri-state option for VCLK, HSYNC, VSYNC at power-down period, 0: Tri-state at this period, 1: No Tri-state at this period; Bit[6]: Tri-state option for output data at power-down period, 0: Tri-state at this period, 1: No Tri-state at this period; Bit[5:0]: Reserved.
3fh	OFF_MUX OFFSET_MO	8	90h	Bit[7]: Gamma Offset Control2, 0: Manual offset2, 1: Auto offset2; Bit[6:0]: The manual written gamma offset.
40h	K0	8	28h	Gamma Correction Slop Coefficients 0.
41h	K1	8	28h	Gamma Correction Slop Coefficients 1.
42h	K2	8	30h	Gamma Correction Slop Coefficients 2.
43h	K3		29h	Gamma Correction Slop Coefficients 3.
44h	K4	8	23h	Gamma Correction Slop Coefficients 4.
45h	K5	8	1bh	Gamma Correction Slop Coefficients 5.
46h	K6	8	17h	Gamma Correction Slop Coefficients 6.
47h	K7	8	0fh	Gamma Correction Slop Coefficients 7.
48h	K8	8	0ch	Gamma Correction Slop Coefficients 8.
49h	K9	8	0bh	Gamma Correction Slop Coefficients 9.
4ah	COM12	8	0ch	Bit[7:6]:Reserved. Bit[5:4] 1x: The value of V-blank is {DM_LNH,DM_LNL[7:0]}+4, 00: The value of V-blank is 4, 01: The value of V-blank is{DM_LNH,DM_LNL[7:1]}+4, Bit[3]: Reserved; Bit[1]: Windowing Control, 0: Normal output (default value), 1: Enables Windowing; Bit[0]: Reserved.
4bh	K10	8	09h	Gamma Correction Slop Coefficients 10.
4ch	K11	8	08h	Gamma Correction Slop Coefficients 11.
4eh	K12	8	07h	Gamma Correction Slop Coefficients 12.
4fh	K13	8	05h	Gamma Correction Slop Coefficients 13.



50h	K14	8	04h	Gamma Correction Slop Coefficients 14.
55h	BRIGHT	8	00h	Brightness Control: Bit[7]: 0: Positive, 1: Negative; Bit[6:0]: Value.
56h	Y_COEF	8	40h	Y Coefficient for Contrast.
60h	MA_TH_CTR1	8	e5h	Bit[7:4]: The threshold1 for judging black sun, Bit[3:0]: The threshold2 for judging black sun.
61h	MA_TH_CTR2	8	48h	Bit[7]: Black Sun Edge Control, 0: don't care about the black sun edge, 1: care about the black sun edge; Bit[6]: Reserved; Bit[5:0]: Threshold for judging black sun edge.
65h	G_COEF	8	46h	Lens shading correction gain of G pixel.
66h	B_COEF	8	46h	Lens shading correction gain of B pixel.
67h	MANU	8	80h	Reserved;
68h	MANV	8	80h	Reserved;
69h	DICOM1	8	00h	Dither Control 1, Bit[7]: YCbCr RANGE Selection, 0: Y/CB/CR: 0~255, 1: Y: 16~235, CB/CR: 16~240; Bit[6]:Reserved; Bit[5]:Reserved; Bit[4]: U、V Dither when in YCbCr Mode/B、R Dither when in RGB Mode: 0: Low 2 bits, 1: Low 3 bits; Bit[3]: Y Dither when in YCbCr Mode/G Dither when in RGB Mode: 0: Low 2 bits, 1: Low 3 bits; Bit[2]: Y dither enable/G dither enable; Bit[1]: U、V dither enable/B、R dither enable; Bit[0]:Reserved;
6ah	GNGAINREG	8	81h	Bit[7:3]: Reserved; Bit[2:0]: G Channel Gain (Bit[2:0] is used as GreenGain[5:3]).
6bh	COM9	8	42h	Bit[7]: 0: Select column gate subsample for CK-GATE subsample, 1: Select HREF for CK-GATE subsample; Bit[6]: CCIR656 Control, 0: Disable CCIR656, 1: Enable CCIR656; Bit[5:4]: Average Weight Selection; Bit[3]: 0: Normal, 1: CK-GATE is ahead 1 of MCLK(YUV) or PCLK(Raw Data); Bit[2]: 0: Normal, 1: CK-GATE is ahead 0.5 of MCLK(YUV) or PCLK(Raw Data); Bit[1]: 0: no CK-GATE when HREF=0, 1: always has CK-GATE; Bit[0]: 0: Disable CK-GATE subsample, 1: Enable CK-GATE subsample.
6dh	INT_TIM_TH	8	20h	INT_TIM Compare Mark Bit[7]: 0: Care about the scene for black sun detection, 1: Don't care about the scene for black sun detection; Bit[6:0]: The threshold of integration time for black sun detection.
6fh	DICOM2	8	7fh	Bit[7]: 0: Enable PRE_DATFOR, 1: Disable PRE_DATFOR; Bit[6:0]: Y threshold for dither.
70h	INTCTR	8	0fh	Interpolation Control, Bit[7]: Edge De-noise outdoor Control, 0: Enable edge de-noise outdoor, 1: Disable edge de-noise outdoor; Bit[6:4]:Reserved; Bit[3]: Edge Enhancement Control, 0: Disable edge enhancement, 1: Enable edge enhancement; Bit[2]: Output Raw Data Selection, 0: Output Raw Data processed by bad pixel correction and de-noise, 1: Output Raw Data without any ISP; Bit[1]: Reserved; Bit[0]: De-noise Control, 0: Disable de-noise, 1: Enable de-noise.

71h	BPCCTR	8	46h	Bit[7:4]: Threshold for bad pixel detection; Bit[3:0]: Threshold for judging whether it is a bad region.
72h	DENCTR	8	2fh	Bit[7:4]: Base threshold for de-noise; Bit[3:0]: Threshold1 for flat field.
73h	EDGCTR	8	2fh	Bit[7:4]: Based value for edge modification; Bit[3:0]: Threshold for edge detection.
74h	DAECTR	8	27h	Bit[7]: Black Sun Correction of Last Frame Control, 0: Disable black sun correction of last frame, 1: Enable black sun correction of last frame; Bit[6:4]: Reserved; Bit[3:0]: Default global gain threshold for de-noise.
75h	EFFCTR	8	12h	Bit[7]: Sram Control, 0: Enable SRAM, 1: Disable SRAM; Bit[6:4]: Positive Edge Enhancement Gain, 000: 0.5, 001: 1.0, 010: 1.5, 011: 2.0, 100: 2.5, 101: 3.0, 110: 3.5, 111: 4.0 ; Bit[3]: Edge Compensation Mode Selection: 0: Auto, 1: Manual; Bit[2:0]: Negative Edge Enhancement Gain, 000: 0.5, 001: 1.0, 010: 1.5, 011: 2.0, 100: 2.5, 101: 3.0, 110: 3.5, 111: 4.0 .
76h	SOBCTR	8	10h	Bit[7]: Color Fringe Correction Control, 0: Disable color fringe correction, 1: Enable color fringe correction; Bit[6]: Choose the Value of Edge Maximum, 0: 128, 1: 64; Bit[5]: Color Fringe Correction Mode Selection for Color Correction, 0: Color (blue, purple etc.) edges are selected, 1: All edges are selected; Bit[4]: Thin Edge Control, 0: Disable thin edge, 1: Enable thin edge; Bit[3:0]: Reserved.
79h	BLACTR	8		Bit[7:4]: Y_AVER Threshold for De-noise in Low Light; Bit[3]: Auto De-noise in Low Light Control, 0: Disable auto de-noise in Low Light, 1: Enable auto de-noise in Low Light; Bit[2]: Cluster Correction Control 0: Disable cluster correction, 1: Enable cluster correction; Bit[1]: Data selected for de-noise, 0: Select mean value, 1: Select center pixel; Bit[0]: Edge De-noise Control, 0: Select center pixel for de-noise, 1: Select edge mean for de-noise(no bad pixel).
7ah	GAICTR	8	00h	Bit[7]: The Selected Luminance for De-noise in Low Light, 0: Select luminance of current pixel, 1: Select Y_AVER; Bit[6:0]: Reserved.
7bh	COLCTR	8	55h	Bit[7:4]: The restricted threshold for color fringe correction; Bit[3:0]: The reduced value for color fringe correction.
7ch	SELCTR	8	88h	Bit[7:6]: Parameter1 for de-noise outdoor, 00: 1/64 01: 1/32 10: 1/16 11: 1/8 Bit[5]: Cross Talk Correction Control 1, 0: Disable cross talk correction in vertical direction, 1: Enable cross talk correction in vertical direction; Bit[4]: Cross Talk Correction Control 2, 0: Disable cross talk correction in horizontal direction, 1: Enable cross talk correction in horizontal direction; Bit[3:0]: Parameter2 for de-noise outdoor.

7dh	FLATTH	8	bah	Bit[7:6]: Parameter3 for de-noise outdoor; Bit[5:4]: Parameter1 for Cluster Correction, 00: 1/4, 01: 3/8, 10: 1/2, 11: 3/4; Bit[3:0]: Threshold2 for flat region.
7eh	LOWCTR	8	1ah	Bit[7]: Y_AVER Restricted for de-noise in Low Light Control, 0: Disable Y_AVER restricted for de-noise in low light, 1: Enable Y_AVER restricted for de-noise in low light; Bit[6:5]: Reserved; Bit[4]: Grid Correction Control, 0: Disable grid correction, 1: Enable grid correction; Bit[3:0]: Threshold of Y_AVER restricted for low light.
80h	AE_MODE	8	96h	AE Control Mode, Bit[7]: Reserved; Bit[6]: 0: AE adjusts every two frames; 1: AE adjusts every frame when in dark scene or in bright scene; Bit[5:2]: Reserved; Bit[1]: 0: Select INT_STEP_60 as banding filter value, 1: Select INT_STEP_50 as banding filter value; Bit[0]: Reserved.
81h	AE_SPEED	8	e0h	Bit[7:4]: The speed of AE adjustment from light to dark; Bit[3:0]: The speed of AE adjustment from dark to light.
82h	GLB_MIN1	8	1bh	Global Gain Minimum 1.
83h	GLB_MAX1	8	37h	Global Gain Maximum 1.
84h	GLB_MIN2	8	39h	Global Gain Minimum 2.
85h	GLB_MAX2	8	5dh	Global Gain Maximum 2.
86h	GLB_MAX3	8	77h	Global Gain Maximum 3.
87h	GLB_GAIN0	8	READ ONLY	Global Gain for sensor.
88h	Y_AVER	8	READ ONLY	Y_AVER value.
89h	INT_MAX_MID	8	7d	Bit[7:3]: Maximum integration time; Bit[2:0]: INT_MID.
8ah	(COM8[3]=0) INT_STEP_50 (COM8[3]=1) GAIN_BEG_0	8	99h	(COM8[3]) 0: 50HZ Banding Filter Value low 8 bits, the high 1 bit at register 0x13[4]. (COM8[3]) 1: GAIN_BEG_0.
8bh	(COM8[3]=0) INT_STEP_60 (COM8[3]=1) GAIN_END_0	8	7fh	(COM8[3]) 0: 60HZ Banding Filter Value low 8 bits, the high 1 bit at register 0x13[5]. (COM8[3]) 1: GAIN_END_0.
8ch	INT_TIM[15:8]	8	01h	Integration time MSB.
8dh	INT_TIM[7:0]	8	cbh	Integration time LSB.
8fh	INT_MIN	8	82h	Bit[7]: 0: The minimum integration time is banding filter value, 1: The minimum integration time is set in the register INT_MIN [6:0].
92h	DM_LNL	8	02h	Dummy line inserted after active line low 8 bits.
93h	DM_LNH	8	00h	Dummy line inserted after active line high 8 bits.
94h	(COM8[3]=0) TAR_BASE0 (COM8[3]=1) GAIN_BEG_2	6	42h	(COM8[3]) 0: bit[7:4]: The threshold for the overexposure pixels judgment; bit[3:0]: Control the start of AE. (COM8[3]) 1: GAIN_BEG_2.
95h	(COM8[3]=0) TAR_BASE1 (COM8[3]=1) GAIN_END_2	8	b0h	(COM8[3]) 0: Parameter1 for Y_AVER modification. (COM8[3]) 1: GAIN_END_2.

96h	(COM8[3]=0) COM2 (COM8[3]=1) GAIN_BEG_3	8	50h	COM8[3] 0: Threshold1 for outdoor scene judgment. (COM8[3]) 1: GAIN_BEG_3
98h	COM1	8	0ah	Bit[7]:Reserved; Bit[6]: Reserved; Bit[5:4]: Exposure Center Window Selection, 00: ROW*12/16, COLUMN*12/16, 01: ROW*10/16, COLUMN*10/16, 10: ROW* 8/16, COLUMN* 8/16, 11: ROW* 6/16, COLUMN* 6/16; Bit[3]: The Speed of Digital Gain, 0 : Slow, 1 : Fast; Bit[2:0]: WEIGHT_SEL, 000: 4/8*center+4/8*border, 001: 5/8*center+3/8*border, 010: 6/8*center+2/8*border, 011: 7/8*center+1/8*border, 100~111: center 100%.
9ah	INT_TIM_TH	8	50h	Threshold2 for outdoor scene judgment.
9bh	YOL_G	8	a4h	The vertical center low 8 bits of G (vertical center).
9ch	XOL_G	8	7ch	The horizontal center low 8 bits of G (horizontal center).
9dh	Gain_OR_Last	8	1bh	Global gain.
b6h	MAN_R	8	80h	Define R value.
b7h	MAN_G	8	80h	Define G value.
b8h	MAN_B	8	80h	Define B value.
b9h	TEST_MODE	8	00h	Bit[7]: 1: Test pattern enable, 0: If bit[6:0] is unequal to 7'd0: overlay mode, Bit[7:0]: 8'h00: BYPASS test pattern Bit[6:5]: 00: output color bar pattern, 01: output gradual pattern, 10: output manual write R/G/B, 11: auto mode, speed controlled by bit[4:0]; Bit[4]: 0: Vertical pattern, 1: Horizontal pattern; Bit[3:0]: Gradual gray pattern mode control.
bbh	BLANK	8	20H	BIT[7:6]: Hsync Delay Control 00: No delay, 01: Delay 2.5ns, 10: Delay 5ns, 11: Delay 9ns; Bit[5]: 0: Disable Xclk deglitch, 1: Enable Xclk deglitch; Bit[4]: Vclk Delay, 0: No delay, 1: Delay 6ns; Bit[3]: Reserved; Bit[2]: CLK_I2C_SYN Delay Selection 0: No delay, 1: Delay 4ns; Bit[1:0]: VCLK Delay Selection, 00: No delay, 01: Delay 2.5ns, 10: Delay 5ns, 11: Delay 9ns.
bch	YOH_R VFLIP_MUX HFLIP_MUX	8	0ch	Bit[7:5]: Reserved; Bit[4]: The vertical center high 1 bit of R; Bit[3]: VFLIP_MUX; Bit[2]: HFLIP_MUX; Bit[1:0]: Reserved.
bdh	YOL_R	8	a4h	The vertical center low 8 bits of R (vertical center).
beh	XOL_R	8	7ch	The horizontal center low 8 bits of R (horizontal center).
dah	H_START_H	8	00h	When register 0x4a[1] is high, analog windowing is enabled, X_WIN_START.
dbh	H_END_H	8	f8h	When register 0x4a[1] is high, analog windowing is enabled, X_WIN_END.

dch	V_START_H	7	00h	When register 0x4a[1] is high, analog windowing is enabled, Y_WIN_START low 8 bits (high 1 bit at VH_ADD_L[0]).
ddh	V_END_H	7	48h	When register 0x4a[1] is high, analog windowing is enabled, Y_WIN_END low 8 bits (high 1 bit at VH_ADD_L[5]).
deh	VH_ADD_L	8	10h	When Register 0x4a[1] is high, analog windowing is enabled, Bit[5]: Y_WIN_END[8]; Bit[0]: Y_WIN_START[8].
e0h	H_HSYNC_EDGE	8	00h	Bit[7:4]: Used to control the rising edge of HSYNC 3 MSB; Bit[3:0]: Used to control the falling edge of HSYNC 3 MSB,
e3h	DM_ROWL	8	06h	Dummy line inserted before active line low 8 bits.
e4h	DM_ROWH	8	00h	Dummy line inserted before active line high 8 bits.
e5h	ISP_CK_PDN_F	8	1eh	Used to control the falling edge of the signal (ISP_CK_PDN), which is for ISP Clock power down.
e6h	ANALOG_PDN_F	8	19h	Used to control the falling edge of the signal (ANALOG_PDN), which is for Analog Clock power down.
e7h	ISP_CK_PDN_R	6	06h	Used to control the rising edge of the ISP_CK_PDN.
efh	SKIN_CTR	8	0bh	Bit[7]: 0: Disable A light signing function, 1: Enable A light signing function; Bit[6]: 0: Disable white pixels signing function, 1: Enable white pixels signing function; Bit[5:4]: Reserved; Bit[3]: 0: Disable skin function, 1: Enable skin function; Bit[2]: 0: Disable hue rotate, 1: Enable hue rotate; Bit[1:0]: 0x: Display full resolution and can do hue with full resolution, 10: Only display skin area and only can do hue with skin area, 11: Display full resolution but only can do hue with skin area.
f1h	BYPASS0	8	00h	Bit[7]: Data Format Enable, 0: Enable, 1: Disable; Bit[6]: Contrast Enable, 0: Enable, 1: Disable; Bit[5]: Reserved; Bit[4]: Color Space & Color Correction Enable, 0: Enable, 1: Disable; Bit[3]: Reserved; Bit[2]: Color Interpolation Enable, 0: Enable, 1: Disable; Bit[1]: Gamma Correction Enable, 0: Enable, 1: Disable; Bit[0]: Lens Shading Correction Enable, 0: Enable, 1: Disable.
f8h	HUE_COS	8	7fh	Hue cosine coefficient range: -1~0.99(0X80~0X7F), MSB is symbol.
f9h	HUE_SIN	8	00h	Hue sine coefficient range: -1~0.99(0X80~0X7F), MSB is symbol.
fch	PID_Semiconductor	8	39h,RO	Product ID MSB, Read Only .
fdh	VER_Semiconductor	8	01h,RO	Product ID LSB, Read Only .

8. Package Specifications

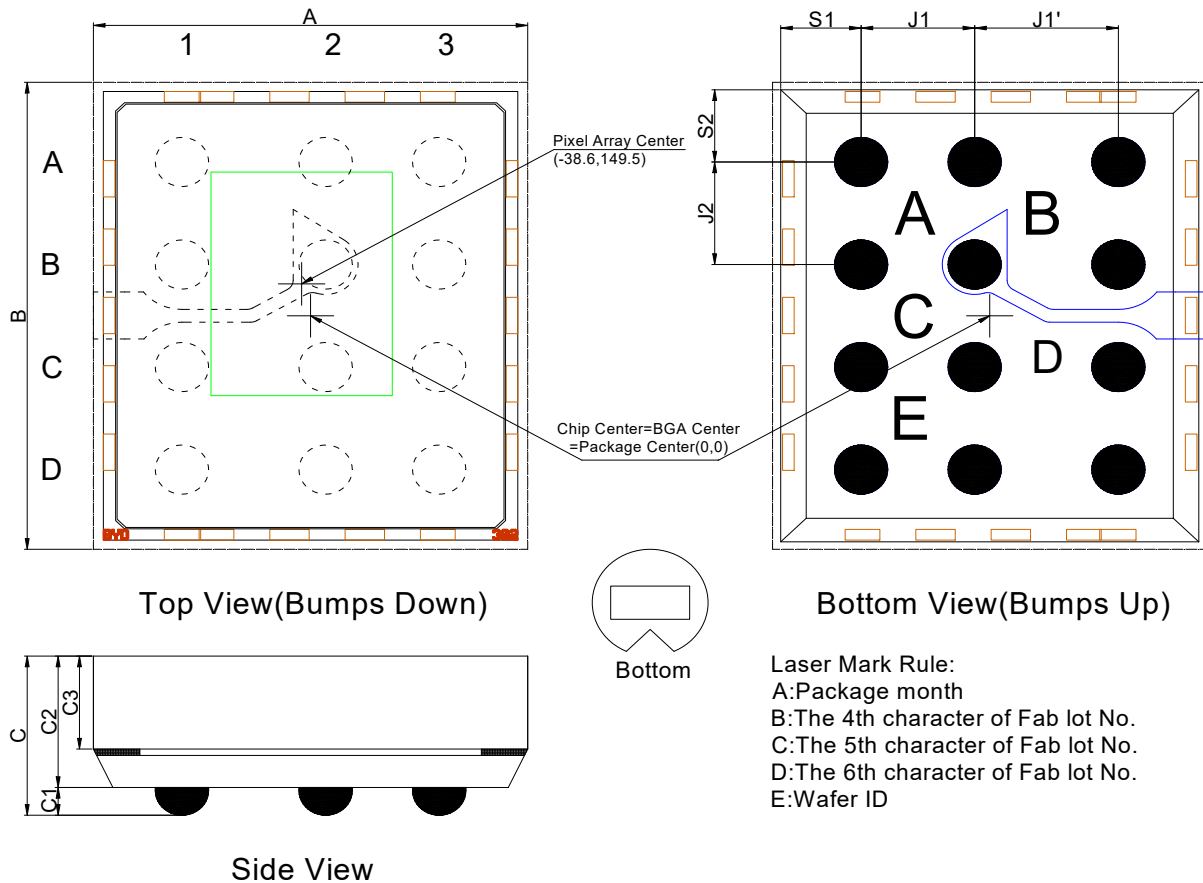


Figure 7 CSP dimension description

Table 6 CSP Dimensions

Description	Symbol	Nominal	Min	Max
		Unit:(mm)		
Package body dimension X	A	1.804	1.779	1.829
Package body dimension Y	B	2.116	2.091	2.141
Package height	C	0.745	0.685	0.805
Ball height	C1	0.130	0.100	0.160
Package body thickness	C2	0.615	0.580	0.650
Thickness from top glass surface to wafer	C3	0.435	0.415	0.455
Ball diameter	D	0.230	0.200	0.260
Total ball count	N	12	-	-
Edge to pin center distance along X	S1	0.382	0.357	0.407
Edge to pin center distance along Y	S2	0.373	0.348	0.398
Ball pitch along X	J1	0.490	0.48	0.50
	J1'	0.620	0.61	0.63
Ball pitch along Y	J2	0.480	0.47	0.49

Table 7 Ball Matrix Table

	1	2	3
A	VDD3A	D3/VSYNC	D0
B	SDA	PDN	D1
C	SCL	XCLK	D2/HREF
D	VSSIO	VDDIO	VCLK

Table 8 Pin Descriptions

Pin Number	Name	Pin type	Function
A1	VDD3A	Power	Power supply.
A2	D3/VSYNC	Output	YUV/RGB image data output port [3] / Vertical sync output.
A3	D0	Output	YUV/RGB image data output port [0].
B1	SDA	I/O	SCCB serial interface data I/O.
B2	PDN	Input(0)*	Power Down Mode Selection. 0: Normal mode.1: Power down mode.
B3	D1	Output	YUV/RGB image data output port [1].
C1	SCL	Input	SCCB serial interface clock input.
C2	XCLK	Input	System clock input.
C3	D2/HSYNC	Output	YUV/RGB image data output port [2] / Horizontal sync output.
D1	GND	Power	Ground..
D2	VDDIO	Power	Power supply for I/O.
D3	VCLK	Output	Pixel clock output.

Note:

** Input(1) represents an internal pull-up resistor.

** Input(0) represents an internal pull-down resistor.

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